Exhibit 4

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

SAMSUNG ELECTRONICS CO., LTD.   )
AND SAMSUNG SEMICONDUCTOR,   )
INC.,   )
)
                Plaintiffs,   )   C.A. No. _____
)
        v.   )
)   **DEMAND FOR JURY TRIAL**
NETLIST, INC.,   )
)
                Defendant.   )

**COMPLAINT FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT AND
UNENFORCEABILITY; BREACH OF CONTRACT**

Plaintiffs Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. (collectively, "Samsung") seek a declaration that Samsung does not directly or indirectly infringe United States Patent Nos. 10,217,523 (the "'523 patent"), 10,474,595 (the "'595 patent"), 9,858,218 (the "'218 patent"), and 7,619,912 (the "'912 patent") (collectively, the "Patents-in-Suit") (Exhibits A-D), either literally or under the doctrine of equivalents; a declaration that the Patents-in-Suit are unenforceable due to inequitable conduct and unclean hands; and a ruling that Defendant Netlist, Inc. ("Netlist") has breached contractual obligations owed to Samsung, including obligations to license its allegedly essential patents to Samsung and its affiliates on reasonable and non-discriminatory ("RAND") terms and conditions, as follows:

NATURE OF THE ACTION

1.   This is an action for a declaratory judgment and breach of contract arising under the patent laws of the United States, Title 35 of the United States Code, the Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.*, and state contract law.

write to the memory devices (20) and compare test patterns read from the memory devices (20) to

the written patterns to identify faults. *Id*. at 5:28–34, 9:22–42.

36.   Figure 3 provides additional detail regarding the control module, data

handlers and their components and interconnections:

FIG. 3
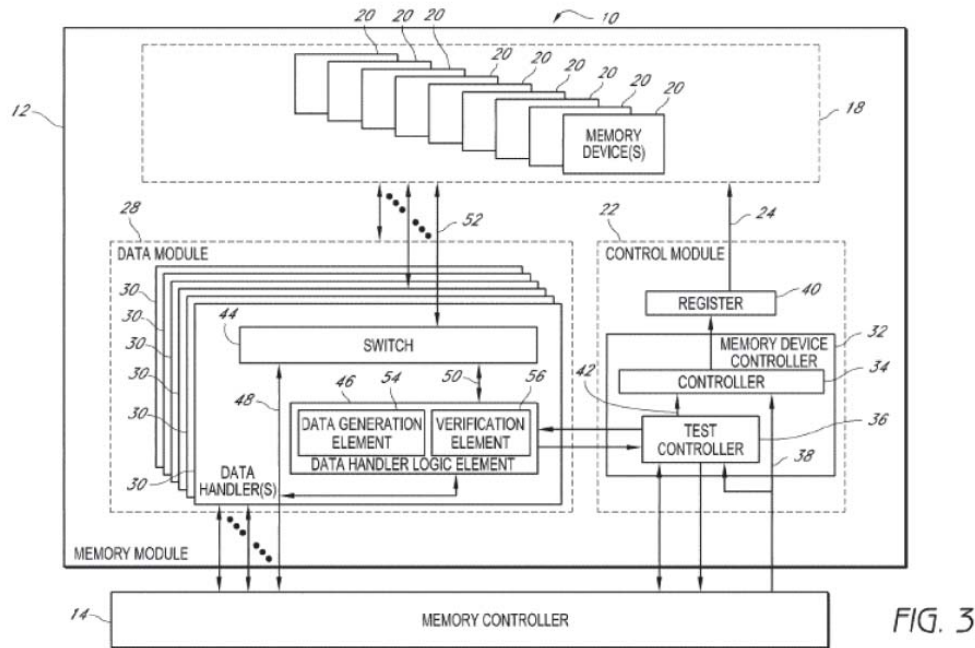
37.   Netlist appears to argue that the DB-to-DRAM Write Delay Training

("MWD Training"), as described in JESD82-32, practices one or more claims of the '523 patent.

According to the standard, "for the DB-to-DRAM write delay training, the MDQ-MDQS delay

adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS

signals with the optimal phase relationship." Ex. E (JESD82-32) at pg. 32. "[T]he data that is

written to the DRAM comes from the data buffer's internal data control words that are written

through the DDR4 register via the BCOM bus." *Id.* The Standard further explains:

> To perform DB-to-DRAM write training, the host will first enable
> the MDQ-MDQS write delay training mode in the Training Mode
> Control Word (BC0C) and it will also program the MPRs F5BC0x
> through F5BC3x and F6BC0x through F6BC3x. After that the host
> sends write commands to an arbitrary DRAM location without

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